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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,033	12/11/2001	Michael S.C. Chung	F0958	6279

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,033	CHUNG, MICHAEL S.C.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,7-12 and 17-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-12 and 17-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: the disclosure "... forces VPP to be regulated to a value given by the equation: VPP1=VREF((C1+C2A)/C1) is misleading because figure 1 of the present application show that the reference voltage (VREF) is compared with voltage (VPPDIV1) corresponding to the ration of capacitors (113) and (114). No multiplication of the reference voltage (VREF) and the ratio of the capacitors is seen. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 17-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 17 the recitations " a switched capacitor" on line 5, "said switched capacitor circuit" on line 6, "said switched capacitor" on lines 10-11 are confusing because it is not clear as to they are the same or different components. The recitation " said switched capacitor comprises two capacitors" is indefinite because it is misdescriptive. A capacitor cannot comprise two capacitors as recited.

Regarding claim 20, the recitation "generating a programming voltage VPP from a **power supply**, wherein said programming voltage is greater than a supply voltage VCC from said power supply" on lines 4-6 is confusing. Figure 1 of the present application shows that voltage (VPP) is generated from the output of the charge pump (101) that receives an oscillating (OCS) from " a ring oscillator" (not shown) thus, the voltage VPP is the boosted voltage of the oscillation voltage (OSC), not the supply voltage. The recitation "activating a

program control signal PGM to enable programming of **a cell of said flash memory**" on lines 7-8 is not clear. Figure 1 shows that the control signal PGM only enables the regulator circuit (104). The "cell of said flash memory" is not shown in the drawing. The recitation "generating a **staircase ramp based** on said programming voltage VPP in response to said program control signal PGM" on lines 9-10 is confusing because the **staircase ramp** (VPP) it self is the "said programming voltage" (VPP). Note that the output voltage (VPP) of the charge pump (101) is programming voltage (VPP) and programming voltage (VPP) is the stair-case ramp. Thus, the recitation "generating a **staircase ramp based** on said programming voltage VPP" is misdescriptive. The Applicant is requested to point out in the drawing the "programming voltage VPP", the "staircase ramp" and to show what is the signal that "enables programming of a cell of said flash memory". The recitation "a clock signal generated by a clock generator and voltage increases corresponding to a reference voltage **times** a ratio of two capacitors" on lines 12-13 is indefinite because it is misdescriptive, According to figure 1 of the present application, the reference voltage (VREF) is applied the negative input of comparator (118) and the positive input of comparator (118) is connected to connecting point of two capacitors (113) and (114). The reference voltage is only compared with voltage (VPPDV1) by comparator (118). The reference voltage is not multiplied with a ratio of two capacitor values as recited.

Claim 18, 19 and 21 are indefinite because of the technical deficiencies of claims 17 and 20.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 7, 8 1-12, and 17-21 are rejected under 35 U.S.C. 102 (e) as being anticipated by Naso et al. (US Pat. 5, 168,174).

Regarding claims 1, 2, figure 3, 4, 5 and 9 shows a circuit for controlling the rise time of a signal comprising: a voltage multiplication circuit (charge pump) for multiplying an input signal; a ramp generator coupled to the multiplication circuit; first and second capacitors (C3, C3) for determining the rise time of said signal; a divide by N counter inherently included in the timer that generates a plurality of clock phases (CKA, CKB). Note that the timer includes clock generator and counter that divide the main clock into a plurality of clock phases (see attached document).

Regarding claim 3, the limitations "...to program and erase Flash EPROM cells" is merely intended use thus, it do not further limit the limitations of the claims. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987). Therefore, these limitations have not been given patentable weight.

Regarding claim 7, the level shift comprises transistor that is connected to the positive input of comparator (COMP1).

Regarding claim 8, two clock signals are (CKA) and (CKB).

Regarding claim 10, the capacitor divider network (C1, C2) or (C3, C4) is coupled to a switched capacitor network (TRy, Cy) in figure 4.

Regarding claims 11 and 12, figures 3 and 4 show that the capacitor divider network switches between ground potential and a node of the divider network (C1, C2) via element (TRx). Comparator (COMP1) is a CMOS comparator.

Regarding claims 17- 19, figure 3, 4, 5 and 9 show a switched capacitor controller comprising: a charge pump; a ramp generator comprising a switch capacitor (Cy); a regulator circuit coupled to the switched capacitor circuit (Cy, C1, C2, C3, C4) that controls the rise time; an oscillator inherently included in the timer for generating clock signal for providing a plurality of clock phases (CKA, CKB). A divider (counter) is inherently included in the timer that generates a plurality of clock phases (CKA, CKB). Note that the timer includes clock

generator and counter that divide the main clock into a plurality of clock phases (see attached document). The capacitor network comprises capacitors (C3) and (C4).

Regarding claims 20 and 21, figures 3, 5 and 9 of Naso show a method of controlling a rise time of an on-chip generated voltage source comprising: generating a programming voltage (Vee); activating a program control signal (SLEN); generating a stair case ramp (Vee) wherein, the period of the steps of the stair case ramp has a period corresponding to a clock signal (CKA) and the rise time depends on the ratio of the capacitor divider (C3, C4). The switched capacitor is capacitor (Cy).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Naso et al. (US Pat. 5, 168,174) in view of Nakahara (US Pat. 6,492,862).

Regarding claim 9, figure 3-5 and 9 of Naso includes all the limitations of claim 9 except for the limitation that the oscillator inherently included in the timer is a ring oscillator. Figure 1 of Nakahara shows a simple ring oscillator circuit comprising inverters for providing a clock signal. Therefore, it would have been obvious to those skilled in the art to replace the oscillator used in the timer with a ring oscillator taught by Nakahara for cost effectiveness.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

03-30-05

TUAN T. LAM
PRIMARY EXAMINER